Lecture 9: Phase-Locked Loop (PLL)

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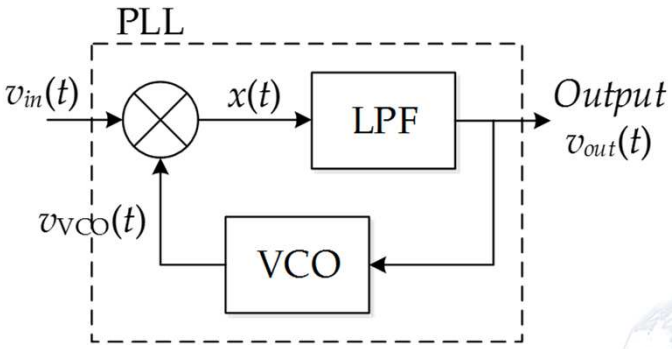
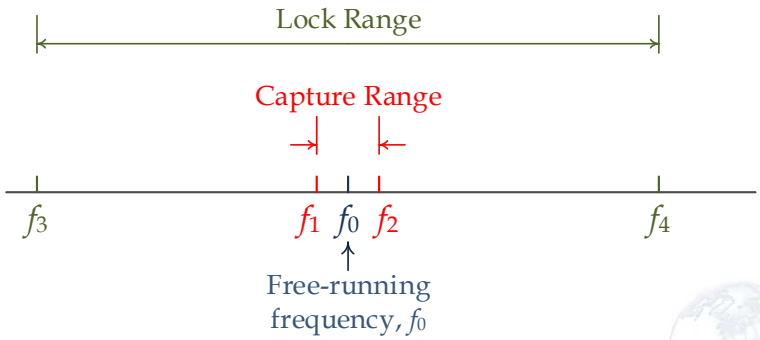
Phase-Locked Loop (PLL)



PLL Characteristics

- **Free-running frequency** f_0.
- **Capture range** or **pull-in range** (between f_1 & f_2).
- **Lock range** or **hold-in range** (between f_3 & f_4).
- Usually lock range is wider than capture range, and free-running frequency is in the middle of both ranges.
- When PLL is **out-of-lock**, the frequency of the inner VCO signal $v_{VCO}(t)$ is equal to the free-running frequency f_0.

PLL Characteristics



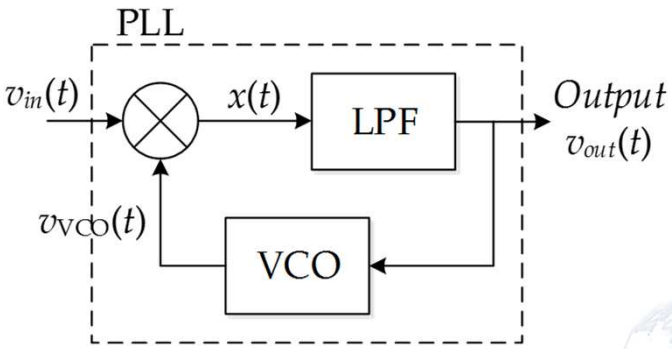
PLL Operations

- Once the frequency of the input signal $v_{in}(t)$ goes within the capture range, the PLL goes into the **in-lock** condition.
- If the PLL stays in-lock, then the frequency of the inner VCO signal $v_{VCO}(t)$ is the *same* as the frequency of the input signal $v_{in}(t)$ (which can be $\varphi_{FM}(t)$).
- If the PLL stays in-lock, then the output voltage $v_{out}(t)$ is proportional to the baseband message signal $m(t)$.
- We want the PLL to stay in-lock.

PLL Terminology

- The PLL stays in-lock so long as the input signal $v_{in}(t)$ frequency is within the lock range.
- If the received signal frequency leaves the lock range, the inner VCO signal $v_{VCO}(t)$ frequency goes back to the free-running frequency (the PLL goes **out-of-lock**).
- See the datasheet for MC4046 for details.

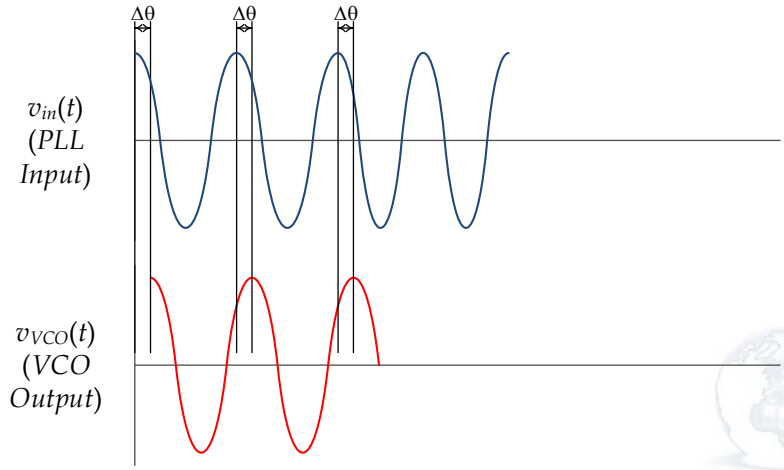
PLL Components & Operation



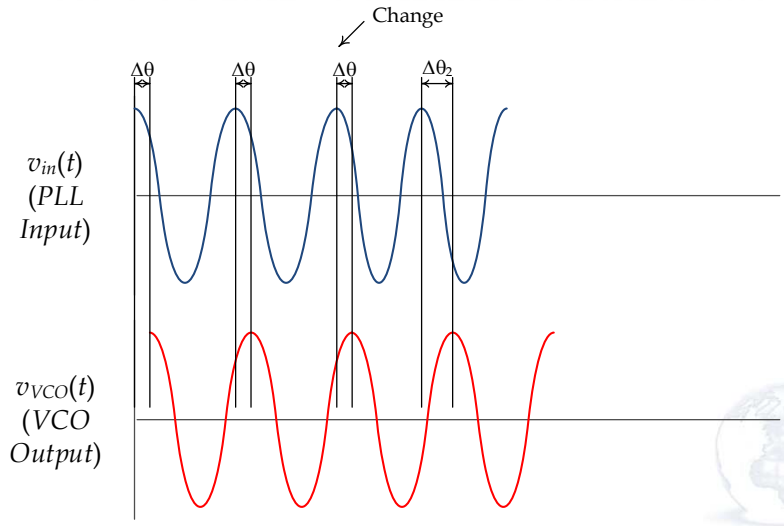
Phase Detector & LPF & VCO

- A phase detector can be built using a multiplication device, which can measure phase difference between two sinusoidal signals.
- After multiplying $v_{VCO}(t)$ and $v_{in}(t)$, the phase detector's output includes both sum and difference frequencies.
- The LPF removes the sum and passes the difference (low frequency), which is then fed back to the VCO.
- The feedback signal controls the inner VCO signal $v_{VCO}(t)$ frequency to match the input signal $v_{in}(t)$ frequency.

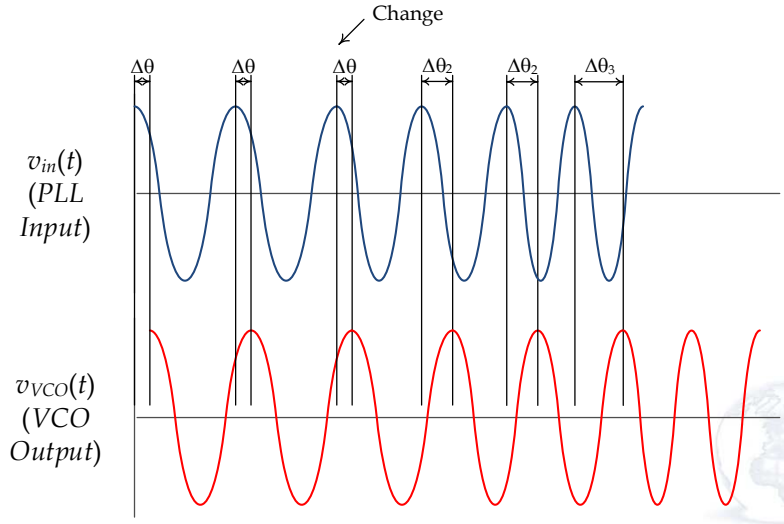
PLL: Step 1 (In Lock)



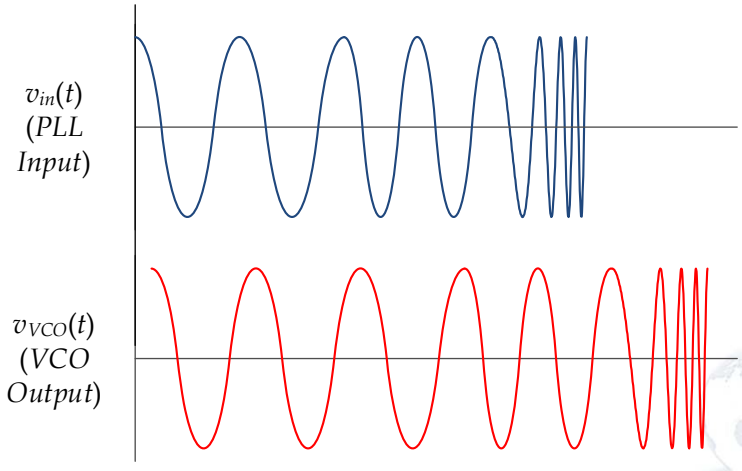
PLL: Step 2 (Input changes)



PLL: Step 3 (PLL follows)



PLL: Continuous Changes



PLL Capture Range

- The LPF bandwidth determines the *capture range*.
- If input signal frequency does not go inside the *capture range* of the PLL in the first place, the VCO remains at the free-running frequency f_0 and the PLL stays out-of-lock.
- This is because when the input signal frequency is close to the free-running frequency, the difference component has small frequency (within the bandwidth of the LPF), and hence, can be fed back to the VCO.
- If the difference frequency is greater than the LPF bandwidth, the LPF removes the difference and prevents a feedback signal to the VCO.

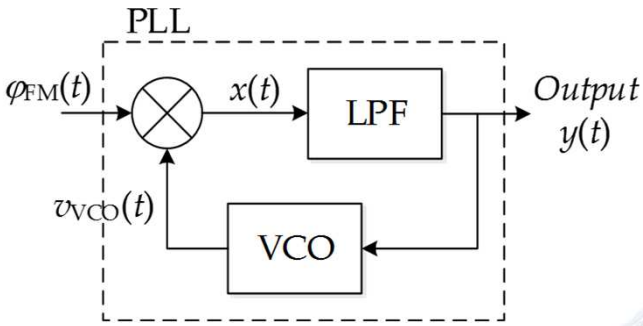
PLL Lock Range

- The lock range depends on the dynamic range of the phase detector's output difference component.
- This is because when the feedback voltage reaches its limit and does not change with an input phase change, it can no longer change the VCO frequency.
- Hence, frequency difference increases between $v_{VCO}(t)$ and $v_{in}(t)$, causing the difference component not to pass through the LPF.
- The VCO frequency then reverts back to the free-running frequency f_0.
- Similarly, the *lock range* depends on the dynamic range of the VCO.

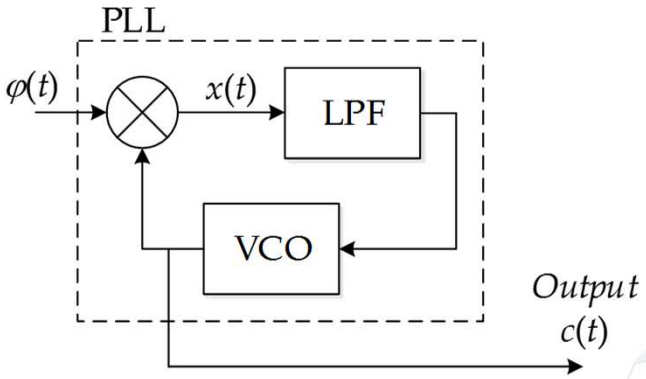
PLL Applications

- FM Demodulator.
- Carrier recovery for synchronous detectors (demodulators).
- Clock recovery for digital baseband receivers (decoders).
- Frequency synthesizers.

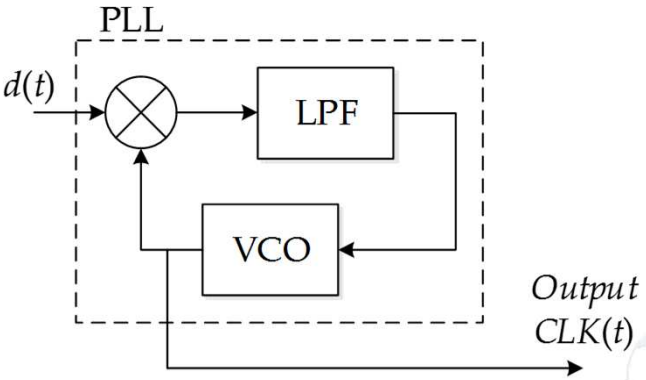
FM Demodulator



Carrier Recovery



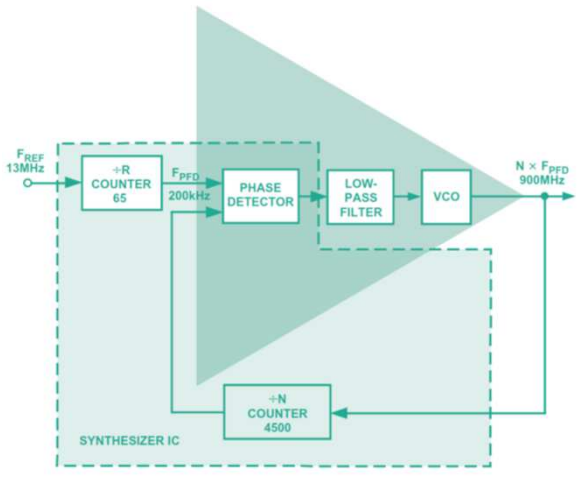
Clock Recovery



Frequency Synthesizer

- A frequency synthesizer can generate a variety of output frequencies as multiples of a single reference frequency.
- High accuracy reference frequency can be generated from a crystal oscillator.
- Crystals can be built at certain constant frequency, e.g., 32 kHz, 4 MHz, 10.7 MHz, 13 MHz, 16.369 MHz, 32 MHz, etc.

Reference to Desired Frequency



Application: Down Converter